11.4 A Digital TV Receiver RF and BB Chipset with Adaptive Bias-Current Control for Mobile Applications

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Digital TV broadcast services aimed at mobile receivers are spreading worldwide. Mobile receivers must be able to cope with adverse reception conditions such as strong adjacent channel interferences and increasing noise levels. In order to accommodate such conditions, mobile receivers must present high linearity and low noise figure. Though this usually results in an increased power consumption of the analog part of the receiver, recent highly linear mobile TV receivers achieve power consumptions as low as 100mW [1].

This paper describes a receiver chipset (Fig. 11.4.1) comprising an RFIC and a baseband IC (BBIC) for ISDB-T 1-segment broadcast, where the reduction of the RFIC power consumption is further exploited by introducing an adaptive bias-current control that is operated by both the RFIC and the BBIC. The RFIC fabricated in a 0.5µm SiGe BiCMOS (Fig. 11.4.7) occupies 3.4×3.4mm^2 and consumes 87mW from a 2.9V supply. Compared to the initial design [2], a power consumption reduction of 45% is already achieved without applying the adaptive control. On the other hand, the BBIC is fabricated in a 0.13µm CMOS (Fig. 11.4.7) and consumes 18mW from a dual supply of 1.2V (core) and 1.8V (I/O).

The bias current of each circuit in the RFIC is designed to provide strong resilience to interferers under PVT variations. In general, characteristics such as gain, linearity, and noise of key blocks of the RFIC degrade as the bias current reduces. However, the gain of the quadrature mixer with cross-coupled transconductor (Fig. 11.4.2) [3] can be kept constant under various bias current settings since the transconductance value of the g_m stage does not depend on the bias current. The measured and simulated performances of the mixer are shown in Fig. 11.4.3. As the bias current decreases, the input-referred noise improves, due to the reduction in the switch current, while the linearity (IIP3) degrades.

The BBIC, shown in Fig.11.4.1, consists of two major blocks, a BB processing block and a forward error correction (FEC) block, together with a unique "adaptive control logic" which controls the cooperative operations between the BBIC and the RFIC. In the BB block, the equalizer (EQ) outputs a 20b I- and Q-axis coordinates of equalized symbols to the FEC block. Additionally, a modulation error ratio (MER) estimate is fed to the adaptive control logic.

The most challenging problem in the adaptive bias-current control is to find the optimum bias current in real time without disturbing the reception. Since ISDB-T uses time interleaving and error correction, error bursts occurring in short periods of time, for example less than a few symbols, are spread out and integrally corrected, resulting in an error-free MPEG2 TS packets. In this work, these characteristics are exploited to determine an optimum bias current. Initially, the BBIC averages the MER over 100 symbols or more and compares the estimated MER with two predetermined thresholds. If the measured MER is larger (smaller) than the upper (lower) threshold, the BBIC initiates the bias-current decreasing (increasing) through adaptive control.

The adaptive control starts with the mixer, followed by IF filter, IF VGA, RF VGA, and PPF. The order is decided according to the respective insensitivity of the NF and gain of each block to bias current variations. This minimizes both the power consumption and the receiver performance deterioration. As described in Fig.11.4.4, the bias current of each circuit in the RFIC is decreased or increased slightly during a test period of one or a few symbols, under the control of the BBIC. Concurrently, the BBIC monitors the corresponding MER. The measured MER is then compared with the upper (lower) threshold. If the MER is larger (smaller) than the upper (lower) threshold, the current is decreased (increased) and the test continues. If the MER is between the two thresholds, the bias current is set to the tested value and the control target shifts to the next subcircuit. Since MER is calculated before the de-interleaving process, it effectively reflects the temporary change of the BB signal quality.

Excessive bias-current reduction results in a deteriorated robustness, especially when strong interferer signals suddenly appear. To overcome this problem, a detect-and-reset mechanism is introduced. The power detector is deployed between RF VGA and mixer. When the detector senses large input signals exceeding a predetermined limit, the RFIC sends a warning to the BBIC using a dedicated 1-bit interferer warning line. Upon receiving the warning, the BBIC immediately initializes the adaptive control process while it sets the predetermined bias current values such as to maximize the RFIC performance in terms of linearity and noise. Since the BBIC resets the bias currents in a few microseconds after receiving the warning, the deterioration by sudden interferer signals is minimized. The BBIC keeps monitoring the interferer warning line level and, if it changes after an adequately long interval, restarts the adaptive control process. Since the operation is controlled by the BBIC only, conflict between the detect-and-reset procedure and the adaptive control or the AGC control is avoided.

The RFIC and BBIC are assembled into a 9×9×1.4mm^3 module together with a UHF filter, decoupling capacitors, and a crystal. The module shows a sensitivity ranging from –109.6 to –105.2dBm over the UHF band with a power consumption of 105mW when the adaptive control is turned off. The performance summary of the module is shown in Fig.11.4.5.

Measurements with enabled adaptive control used four input signal patterns: (a) –90dBm desired signal, (b) –100dBm desired signal, (c) –105dBm desired signal, and (d) –90dBm desired signal with –40dBm interferer (NTSC analog TV signal), –6.14MHz away from the desired signal. The test sequence consists of the successive order of patterns (a), (b), (c), (a), and (d) as shown in Fig.11.4.6. When the proposed adaptive control is used, patterns (a) and (b) present the RFIC power consumption of 59mW and 77mW, reduction of 32% and 11%, respectively, without any error during the test. For (a), the initially measured MER is higher than the upper threshold. Therefore, the RFIC current decreases to the minimum. Since the measured MER is smaller than the lower threshold for (b), the RFIC current increases until the measured MER becomes larger than the lower threshold. Since the measured MER is below the lower threshold for (c), no current reduction takes place. On the transition from (a) to (d), a strong interferer appears and the detect-and-reset mechanism is evoked so that the bias currents of all the RFIC components are reset to their initial values. Furthermore, the chipset performance is tested using captured data provided by the Association for Promotion of Digital Broadcasting (D-Pa) at the locations: (1) metropolitan expressway (moving), (2) the urban area covered with single frequency network (SFN), and stationary. In these conditions, the adaptive control does not deteriorate the reception rates at all while it reduces the power consumption by 15.6mW for (1) and 22.6mW for (2).

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[3] M. Koutani and K. Iizuka, "A High OIP3 Quadrature Mixer using Cross-Coupled Transconductor," *Proc. IEEE CICC*, pp. 345-348, Sept., 2005.

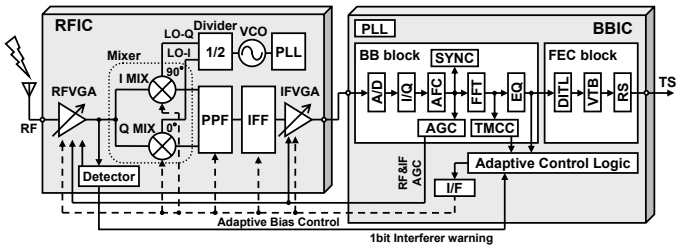


Figure 11.4.1: Block diagram of the receiver.

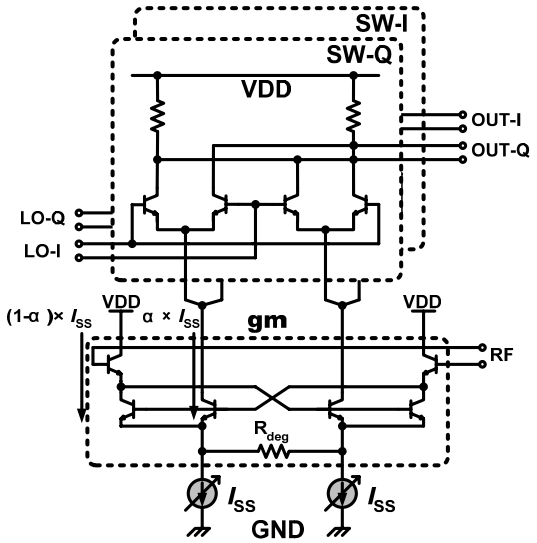


Figure 11.4.2: Schematic of the quadrature mixer with cross-coupled transconductor.

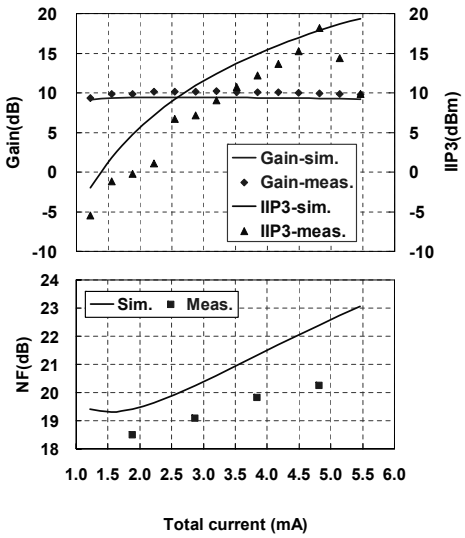


Figure 11.4.3: Total current dependence of measured versus simulated gain, IIP3, and NF for the cross-coupled quadrature mixer.

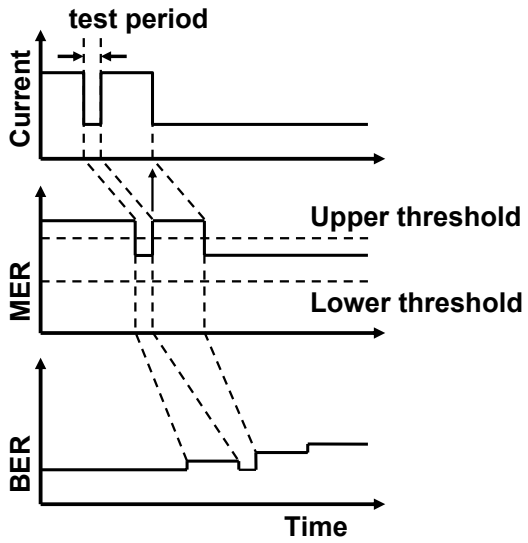
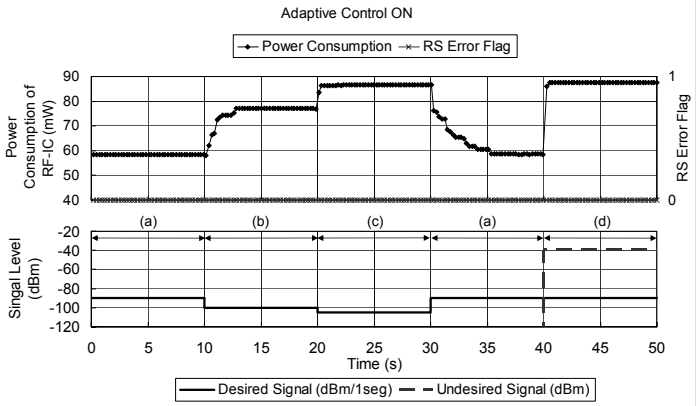


Figure 11.4.4: Adaptive bias current control algorithm.

Frequency Range		UHF 470MHz to 770MHz
Channel Bandwidth		430kHz
Maximum Gain (@13ch)		103dB
NF (@13ch)		2.7dB
Sensitivity (QPSK1/2)		–109.6dBm to – 105.2dBm
Power Consumption with Adaptive Control	BBIC	18mW
	RFIC	59mW to 87mW
	Total (Module)	77mW to 105mW
Supply Voltage(RF/BB Core/BB IO)		2.9V / 1.2 V / 1.8V
Die Size (RF/BB)		3.4×3.4mm² / 4.3×4.3mm²
Technology (RF/BB)		BiCMOS 0.5μm / CMOS 0.13μm

Figure 11.4.5: Performance summary.



RS Error Flag, 0: error free in 256 MPEG2 TS Packets, 1: errors in 256 MPEG2 TS packets

Figure 11.4.6: Measurement result with adaptive control.

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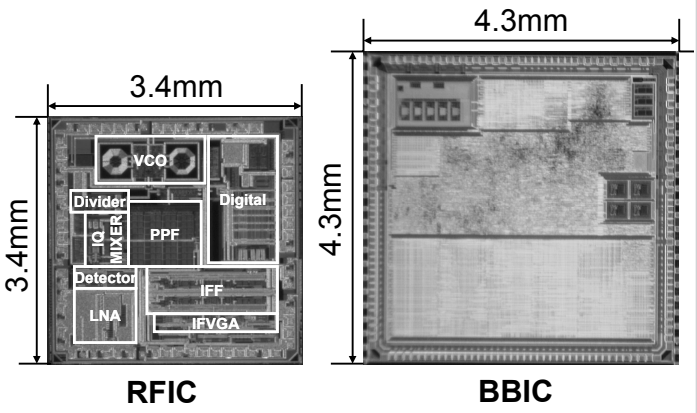

Figure 11.4.7: Chip micrographs.

